FIG.1

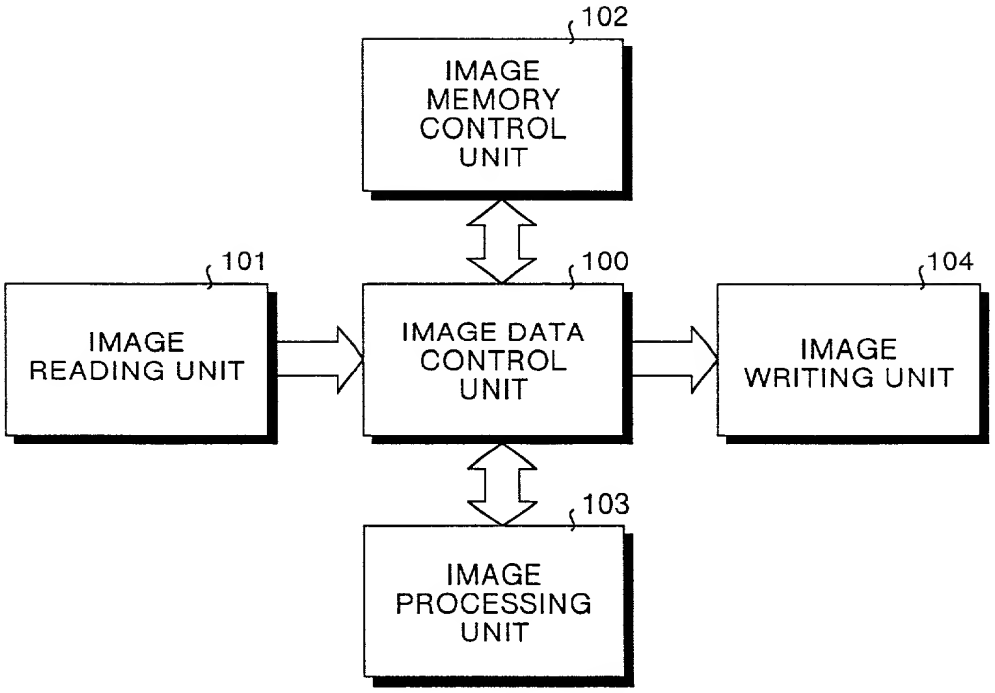

102
IMAGE MEMORY CONTROL UNIT
101
IMAGE READING UNIT
100
IMAGE DATA CONTROL UNIT
104
IMAGE WRITING UNIT
103
IMAGE PROCESSING UNIT

FIG.2

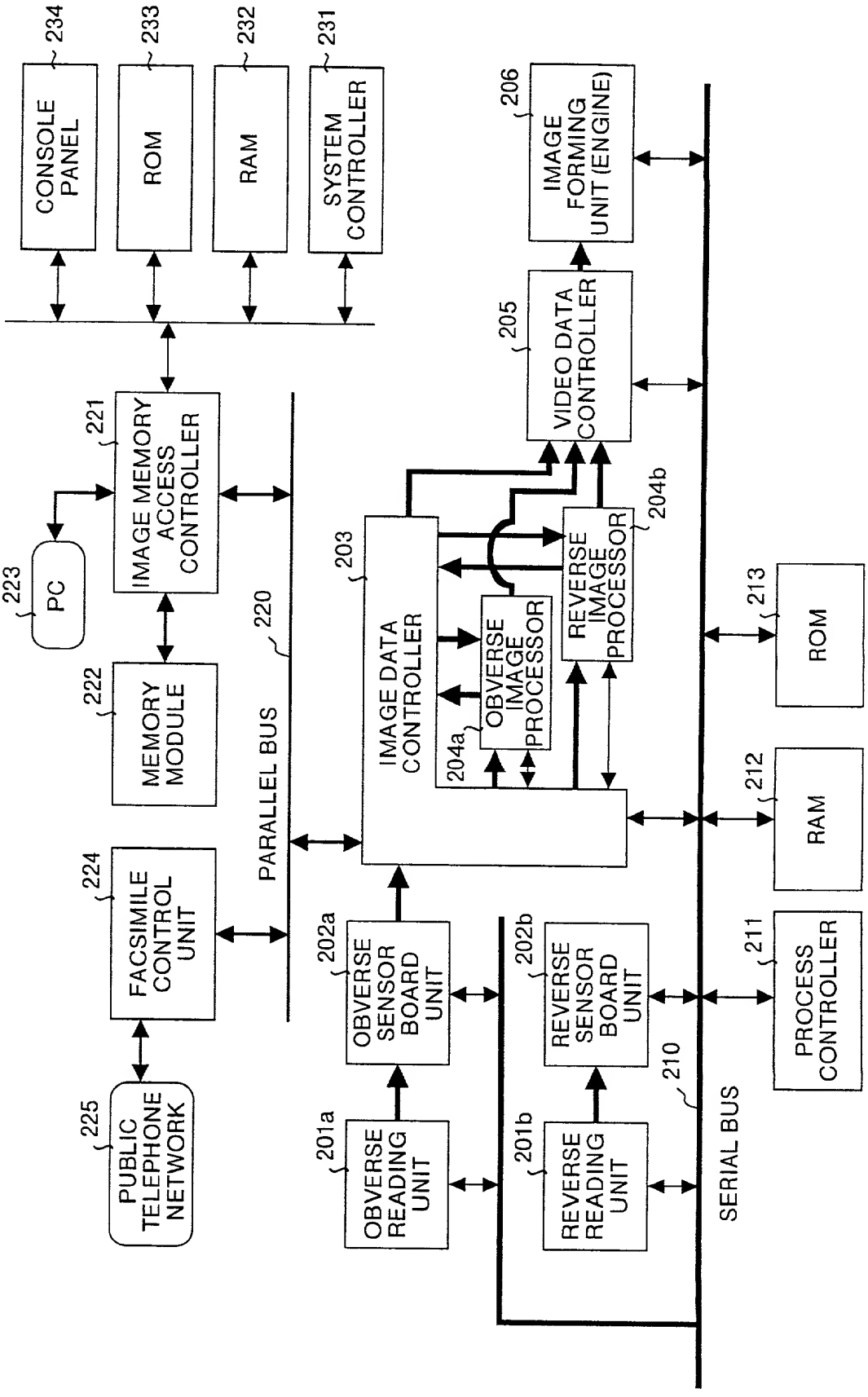

CONSOLE PANEL
234
ROM
233
RAM
232
SYSTEM CONTROLLER
231
IMAGE FORMING UNIT (ENGINE)
206
VIDEO DATA CONTROLLER
205
IMAGE MEMORY ACCESS CONTROLLER
221
PC
223
MEMORY MODULE
222
PARALLEL BUS
220
IMAGE DATA CONTROLLER
203
OBVERSE IMAGE PROCESSOR
204a
REVERSE IMAGE PROCESSOR
204b
ROM
213
RAM
212
FACSIMILE CONTROL UNIT
224
PUBLIC TELEPHONE NETWORK
225
OBVERSE SENSOR BOARD UNIT
202a
REVERSE SENSOR BOARD UNIT
202b
PROCESS CONTROLLER
211
OBVERSE READING UNIT
201a
REVERSE READING UNIT
201b
SERIAL BUS
210

FIG.3

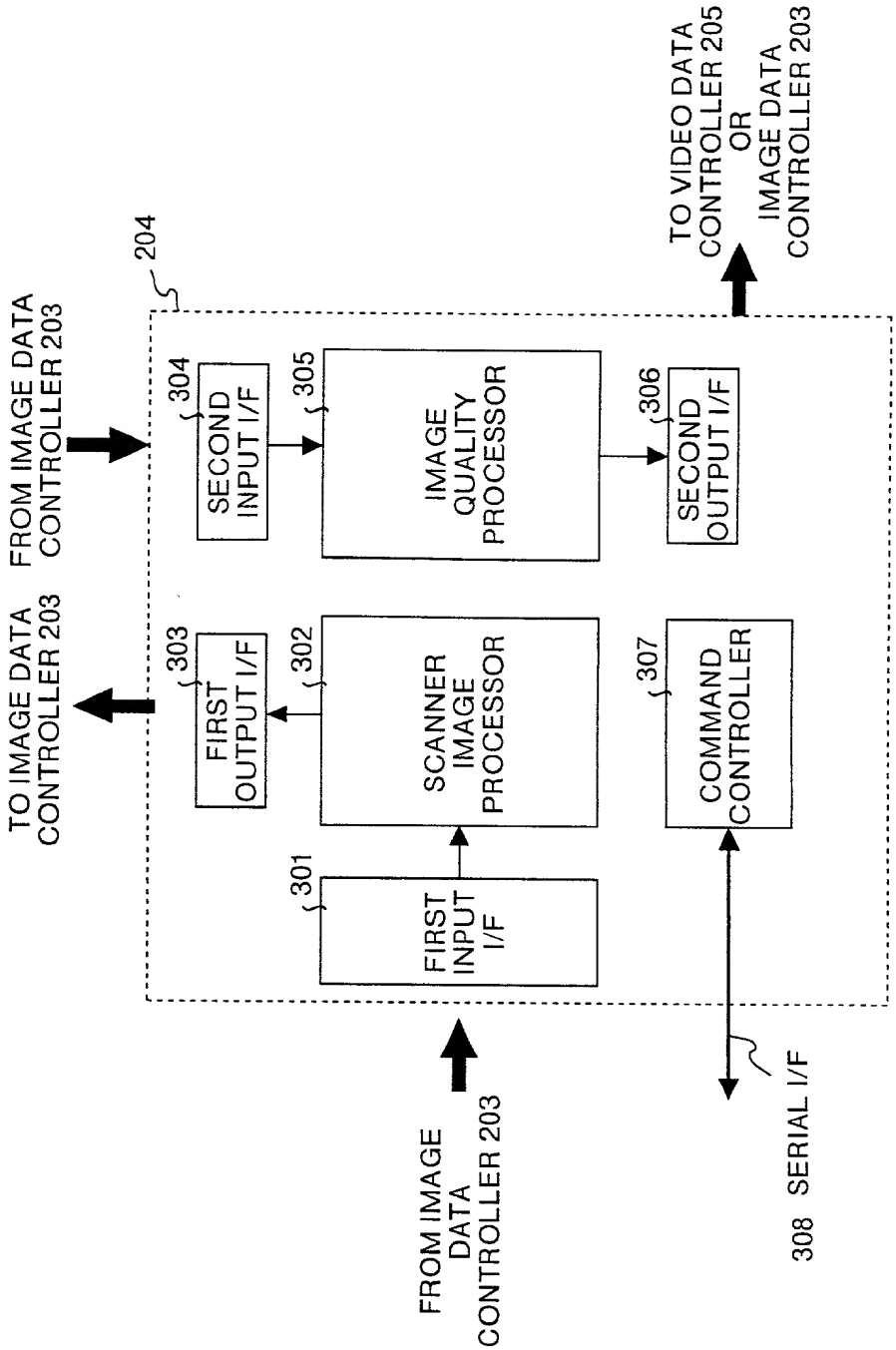

204
FROM IMAGE DATA CONTROLLER 203
TO IMAGE DATA CONTROLLER 203
TO VIDEO DATA CONTROLLER 205 OR IMAGE DATA CONTROLLER 203
FROM IMAGE DATA CONTROLLER 203
308 SERIAL I/F
301 FIRST INPUT I/F
302 SCANNER IMAGE PROCESSOR
303 FIRST OUTPUT I/F
304 SECOND INPUT I/F
305 IMAGE QUALITY PROCESSOR
306 SECOND OUTPUT I/F
307 COMMAND CONTROLLER

FIG.4

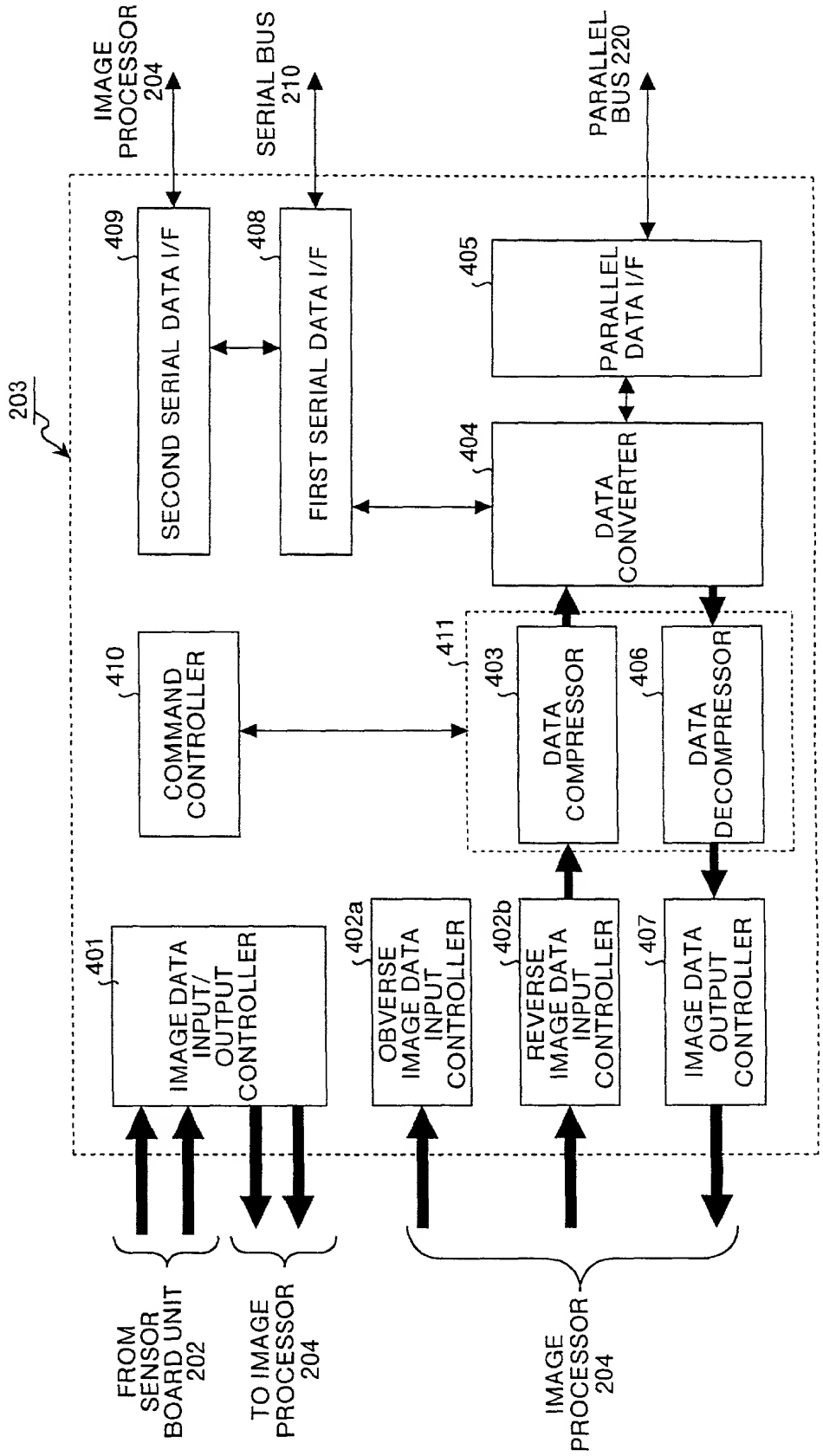


IMAGE PROCESSOR 204
SERIAL BUS 210
PARALLEL BUS 220
203
409
SECOND SERIAL DATA I/F
408
FIRST SERIAL DATA I/F
405
PARALLEL DATA I/F
404
DATA CONVERTER
410
COMMAND CONTROLLER
411
403
DATA COMPRESSOR
406
DATA DECOMPRESSOR
401
IMAGE DATA INPUT/ OUTPUT CONTROLLER
402a
OBVERSE IMAGE DATA INPUT CONTROLLER
402b
REVERSE IMAGE DATA INPUT CONTROLLER
407
IMAGE DATA OUTPUT CONTROLLER
FROM SENSOR BOARD UNIT 202
TO IMAGE PROCESSOR 204
IMAGE PROCESSOR 204

FIG.5

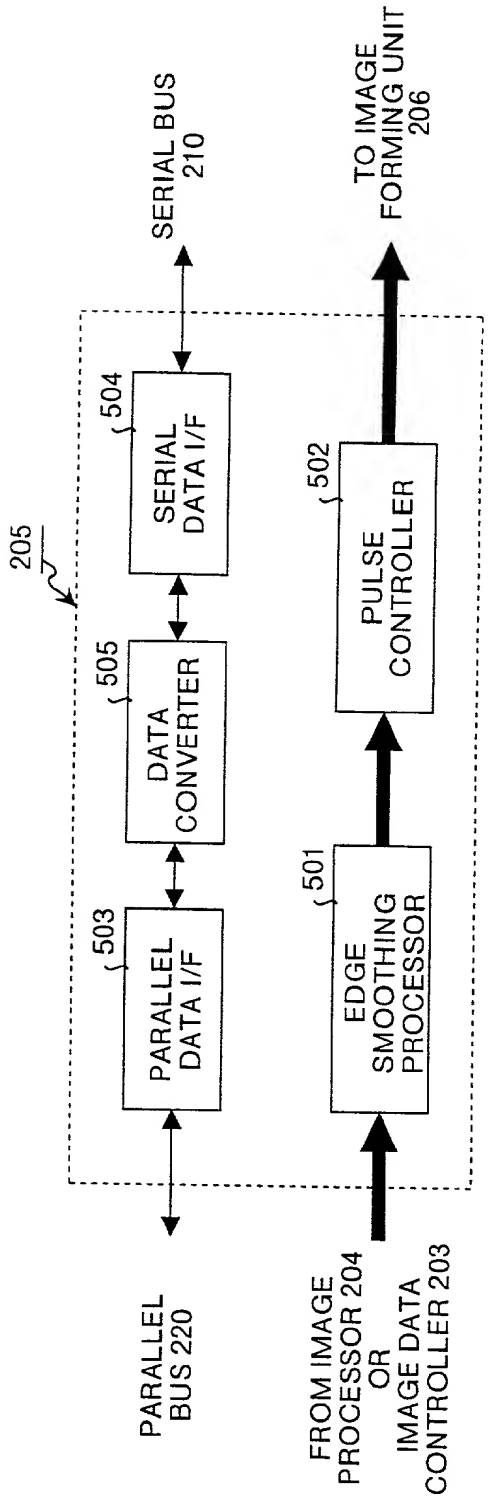

205
SERIAL BUS 210
TO IMAGE FORMING UNIT 206
504
SERIAL DATA I/F
505
DATA CONVERTER
503
PARALLEL DATA I/F
502
PULSE CONTROLLER
501
EDGE SMOOTHING PROCESSOR
PARALLEL BUS 220
FROM IMAGE PROCESSOR 204 OR IMAGE DATA CONTROLLER 203

FIG.6

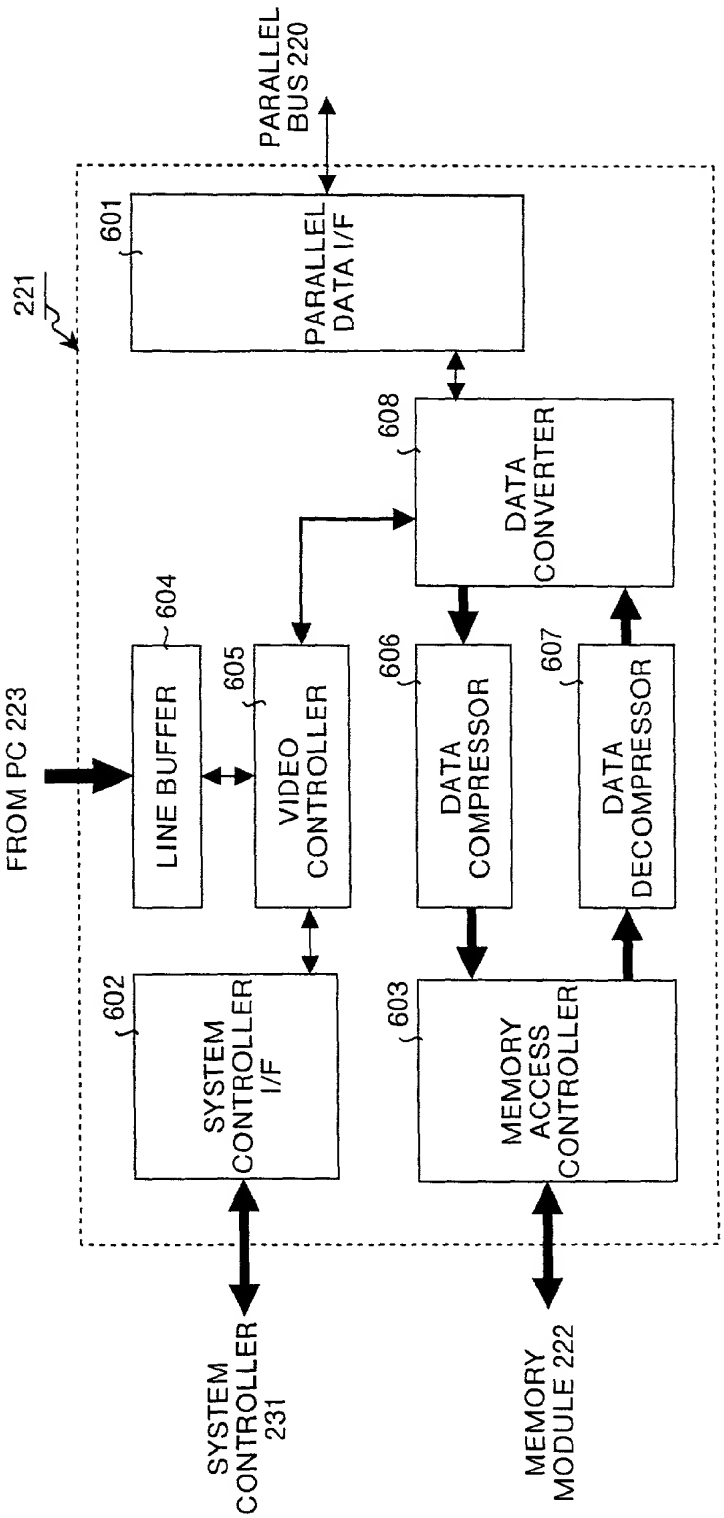

PARALLEL BUS 220
221
601
PARALLEL DATA I/F
608
DATA CONVERTER
604
605
606
607
FROM PC 223
LINE BUFFER
VIDEO CONTROLLER
DATA COMPRESSOR
DATA DECOMPRESSOR
602
603
SYSTEM CONTROLLER I/F
MEMORY ACCESS CONTROLLER
SYSTEM CONTROLLER 231
MEMORY MODULE 222

FIG.7

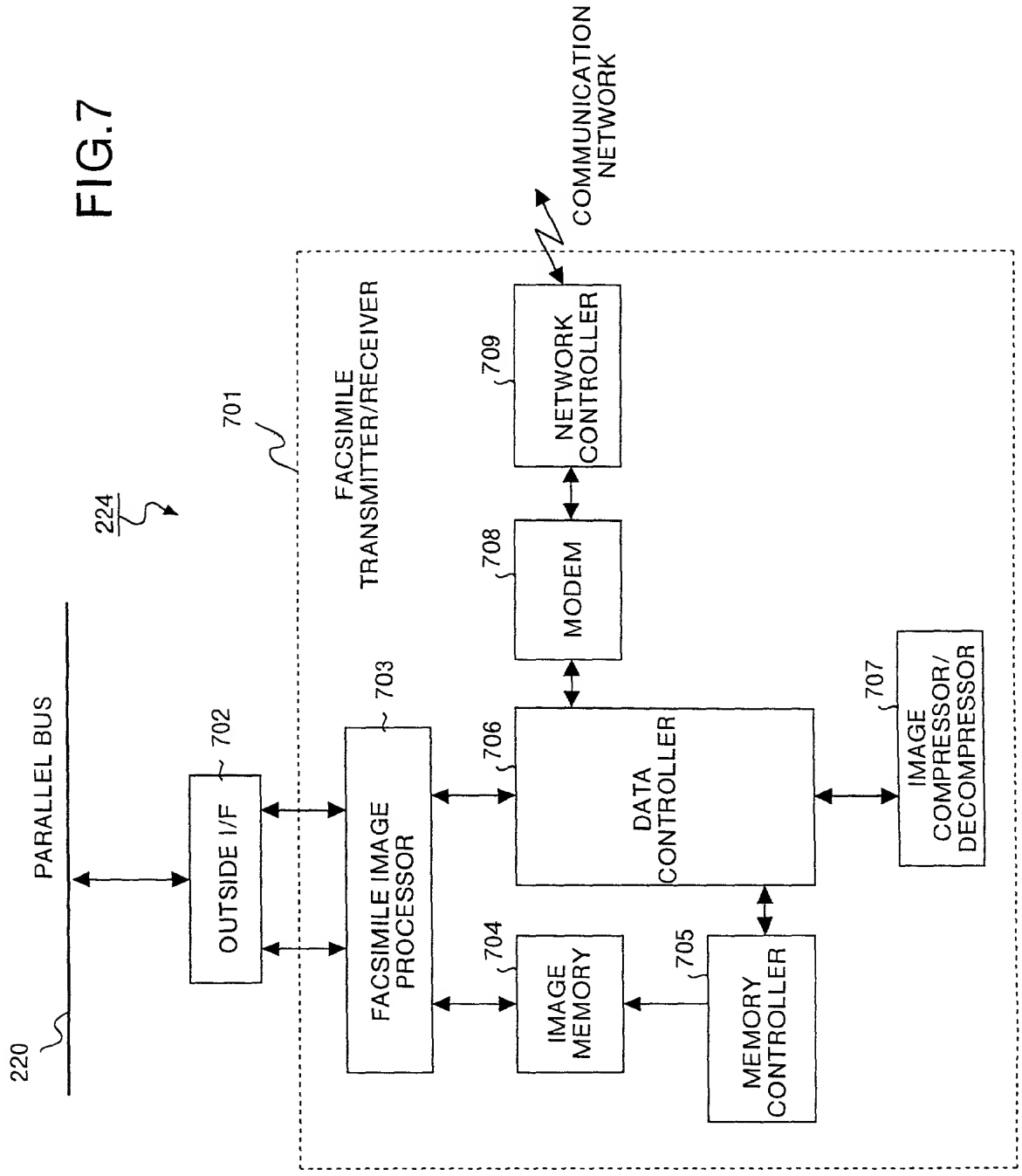

220
PARALLEL BUS
224
701
FACSIMILE TRANSMITTER/RECEIVER
COMMUNICATION NETWORK
OUTSIDE I/F
702
FACSIMILE IMAGE PROCESSOR
703
IMAGE MEMORY
704
MEMORY CONTROLLER
705
DATA CONTROLLER
706
IMAGE COMPRESSOR/ DECOMPRESSOR
707
MODEM
708
NETWORK CONTROLLER
709

FIG.8

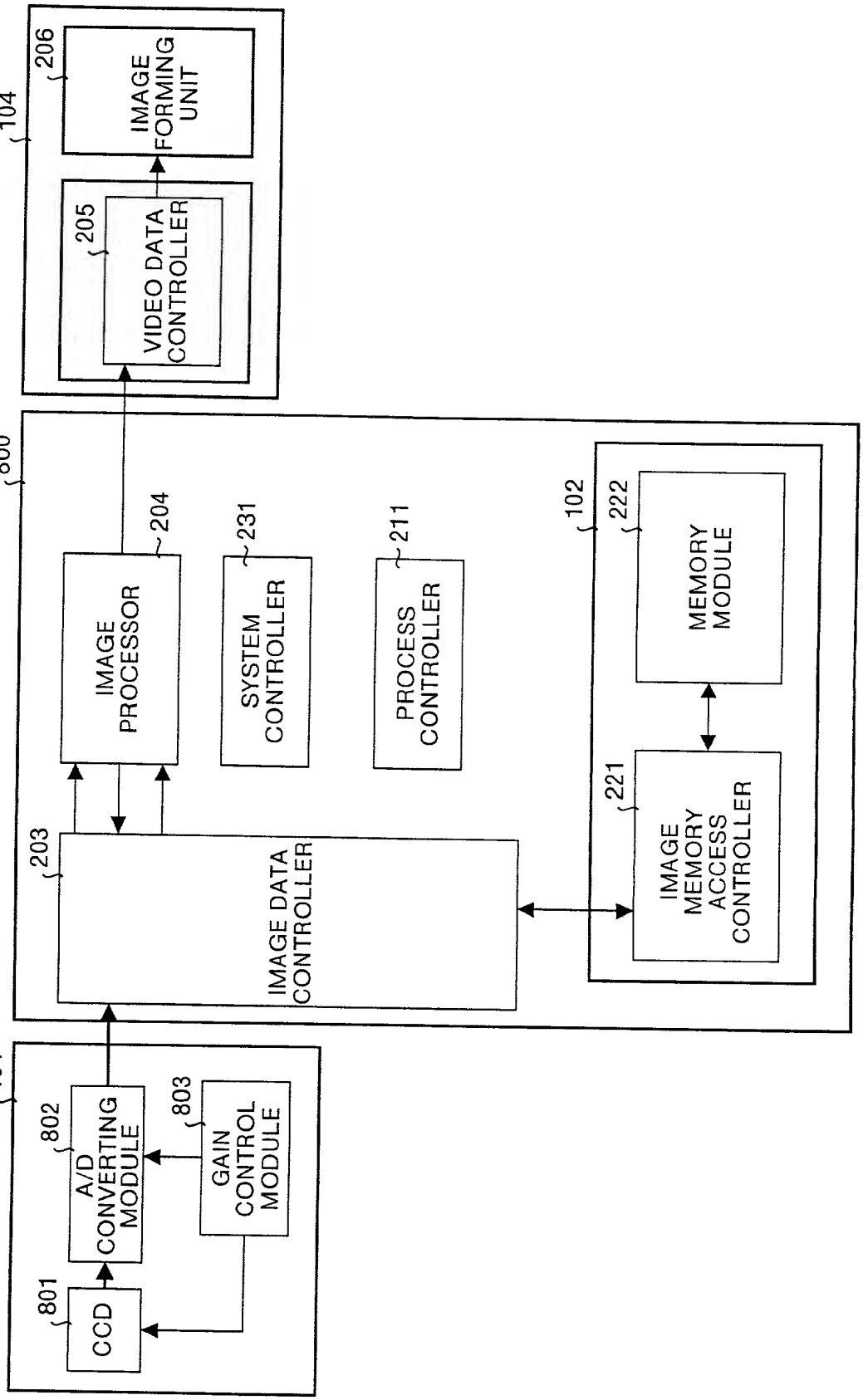

104
206
IMAGE FORMING UNIT
205
VIDEO DATA CONTROLLER
800
204
IMAGE PROCESSOR
231
SYSTEM CONTROLLER
211
PROCESS CONTROLLER
102
222
MEMORY MODULE
203
IMAGE DATA CONTROLLER
221
IMAGE MEMORY ACCESS CONTROLLER
101
802
A/D CONVERTING MODULE
803
GAIN CONTROL MODULE
801
CCD

FIG.9

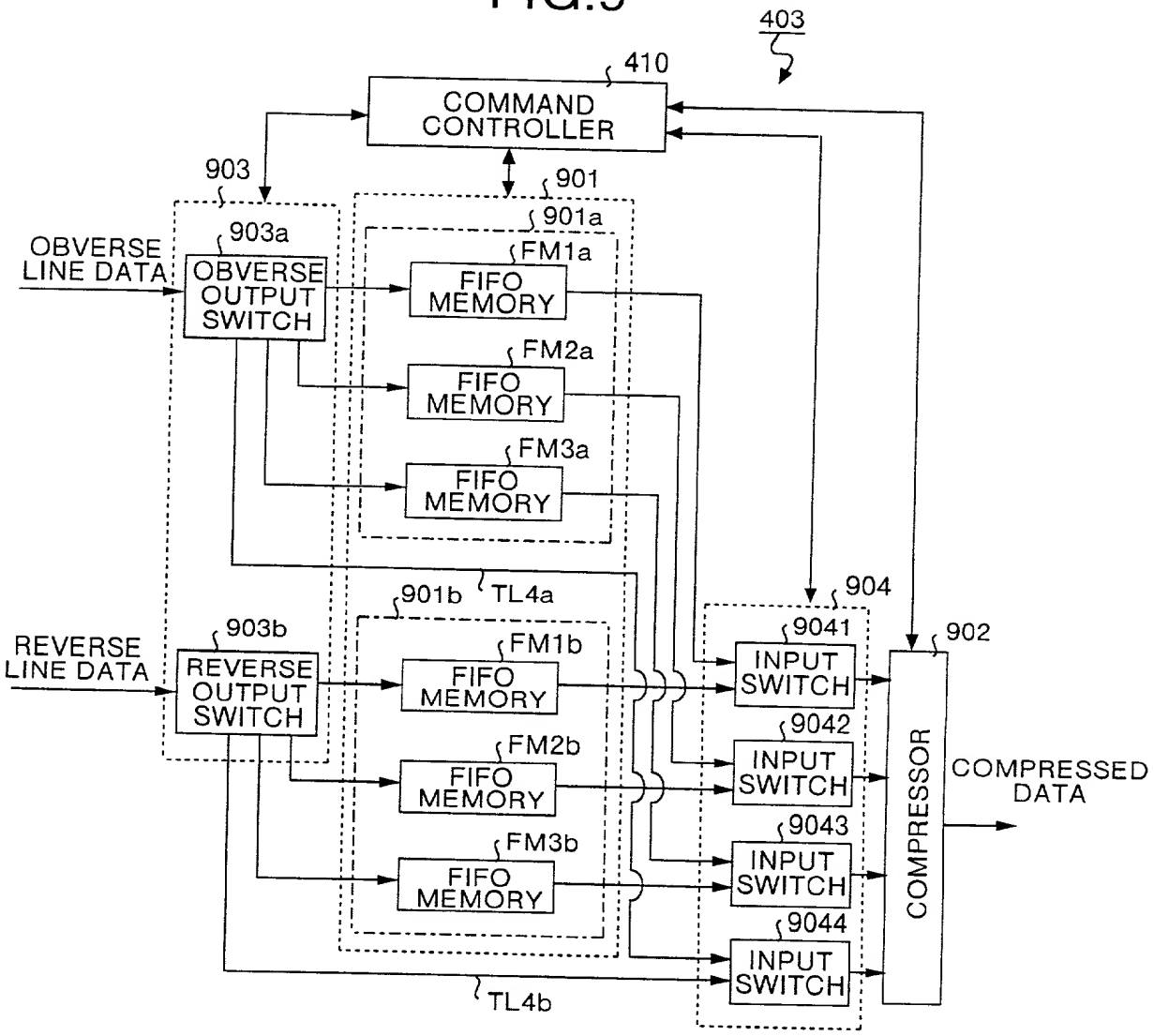

403
410
COMMAND CONTROLLER
903
901
901a
903a
OBVERSE LINE DATA
OBVERSE OUTPUT SWITCH
FM1a
FIFO MEMORY
FM2a
FIFO MEMORY
FM3a
FIFO MEMORY
TL4a
901b
904
903b
REVERSE LINE DATA
REVERSE OUTPUT SWITCH
FM1b
FIFO MEMORY
FM2b
FIFO MEMORY
FM3b
FIFO MEMORY
9041
INPUT SWITCH
9042
INPUT SWITCH
9043
INPUT SWITCH
9044
INPUT SWITCH
902
COMPRESSOR
COMPRESSED DATA
TL4b

FIG.10

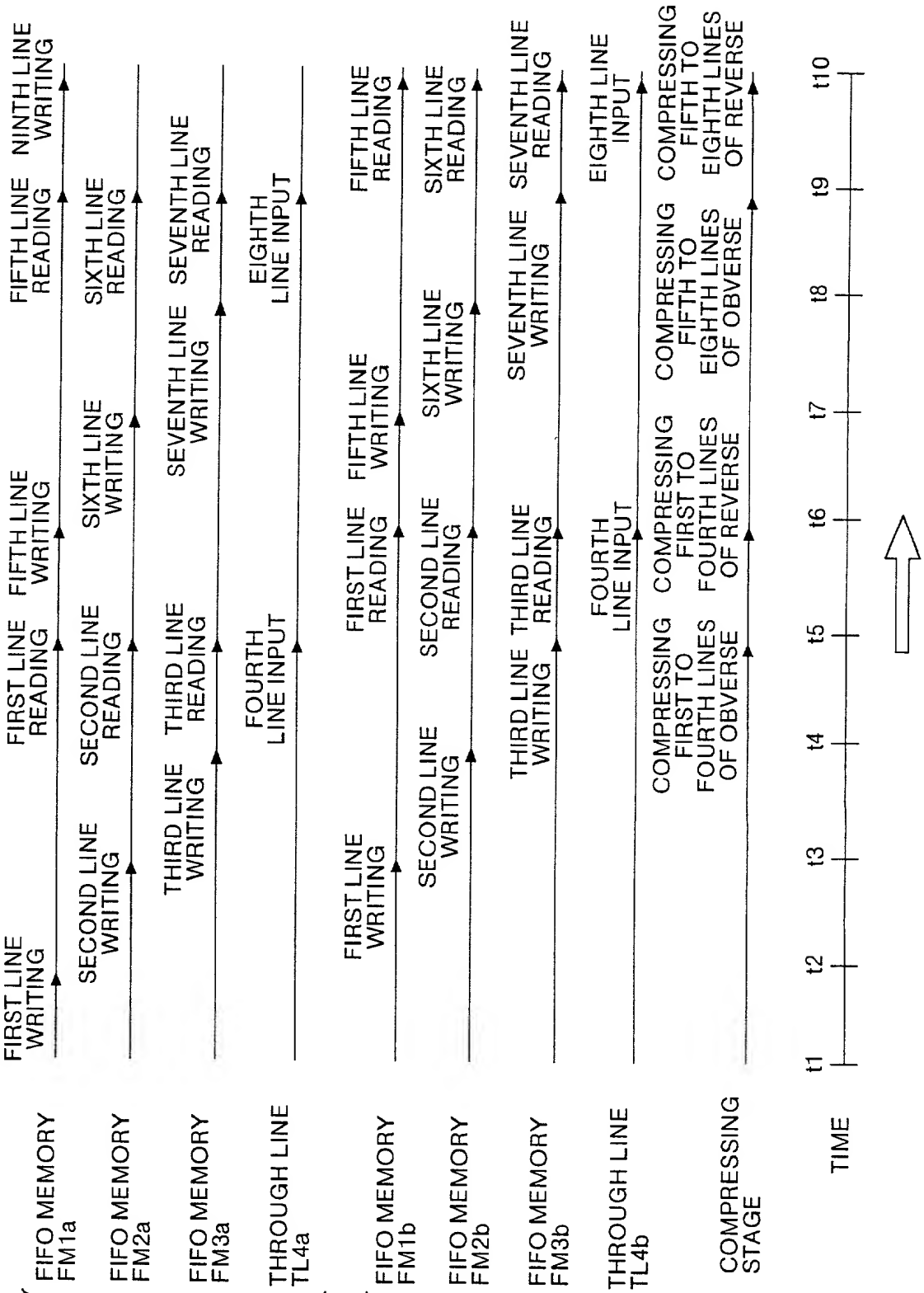

OBVERSE
REVERSE
FIFO MEMORY FM1a
FIFO MEMORY FM2a
FIFO MEMORY FM3a
THROUGH LINE TL4a
FIFO MEMORY FM1b
FIFO MEMORY FM2b
FIFO MEMORY FM3b
THROUGH LINE TL4b
COMPRESSING STAGE
TIME
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
FIRST LINE WRITING
SECOND LINE WRITING
THIRD LINE WRITING
FOURTH LINE INPUT
FIRST LINE READING
SECOND LINE READING
THIRD LINE READING
FIFTH LINE WRITING
SIXTH LINE WRITING
SEVENTH LINE WRITING
EIGHTH LINE INPUT
FIFTH LINE READING
SIXTH LINE READING
SEVENTH LINE READING
NINTH LINE WRITING
COMPRESSING FIRST TO FOURTH LINES OF OBVERSE
COMPRESSING FIFTH TO EIGHTH LINES OF REVERSE

FIG.11

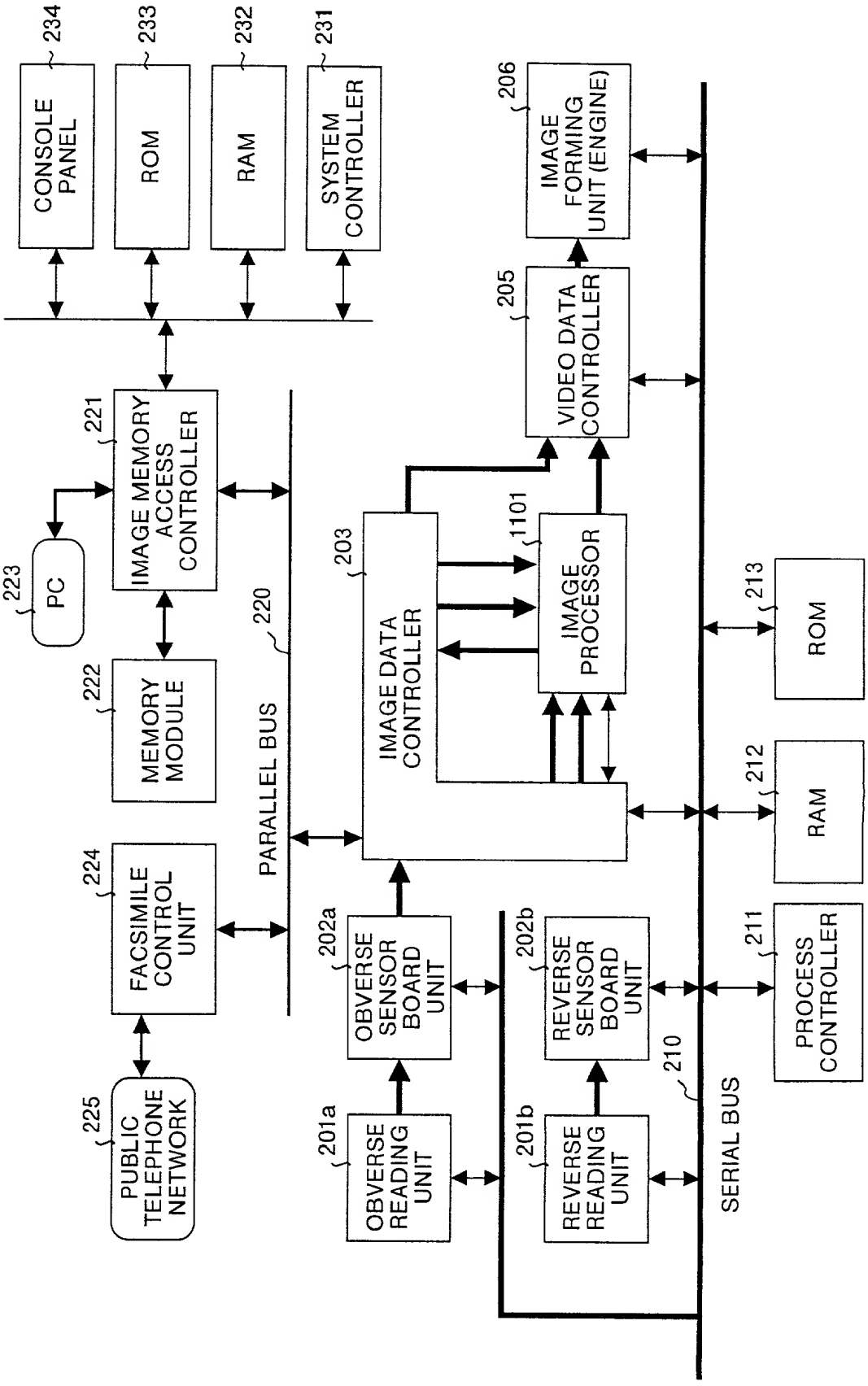

CONSOLE PANEL
234
ROM
233
RAM
232
SYSTEM CONTROLLER
231
IMAGE FORMING UNIT (ENGINE)
206
VIDEO DATA CONTROLLER
205
IMAGE MEMORY ACCESS CONTROLLER
221
PC
223
MEMORY MODULE
222
PARALLEL BUS
220
IMAGE DATA CONTROLLER
203
IMAGE PROCESSOR
1101
ROM
213
RAM
212
FACSIMILE CONTROL UNIT
224
PUBLIC TELEPHONE NETWORK
225
OBVERSE SENSOR BOARD UNIT
202a
REVERSE SENSOR BOARD UNIT
202b
PROCESS CONTROLLER
211
OBVERSE READING UNIT
201a
REVERSE READING UNIT
201b
210
SERIAL BUS

FIG.12

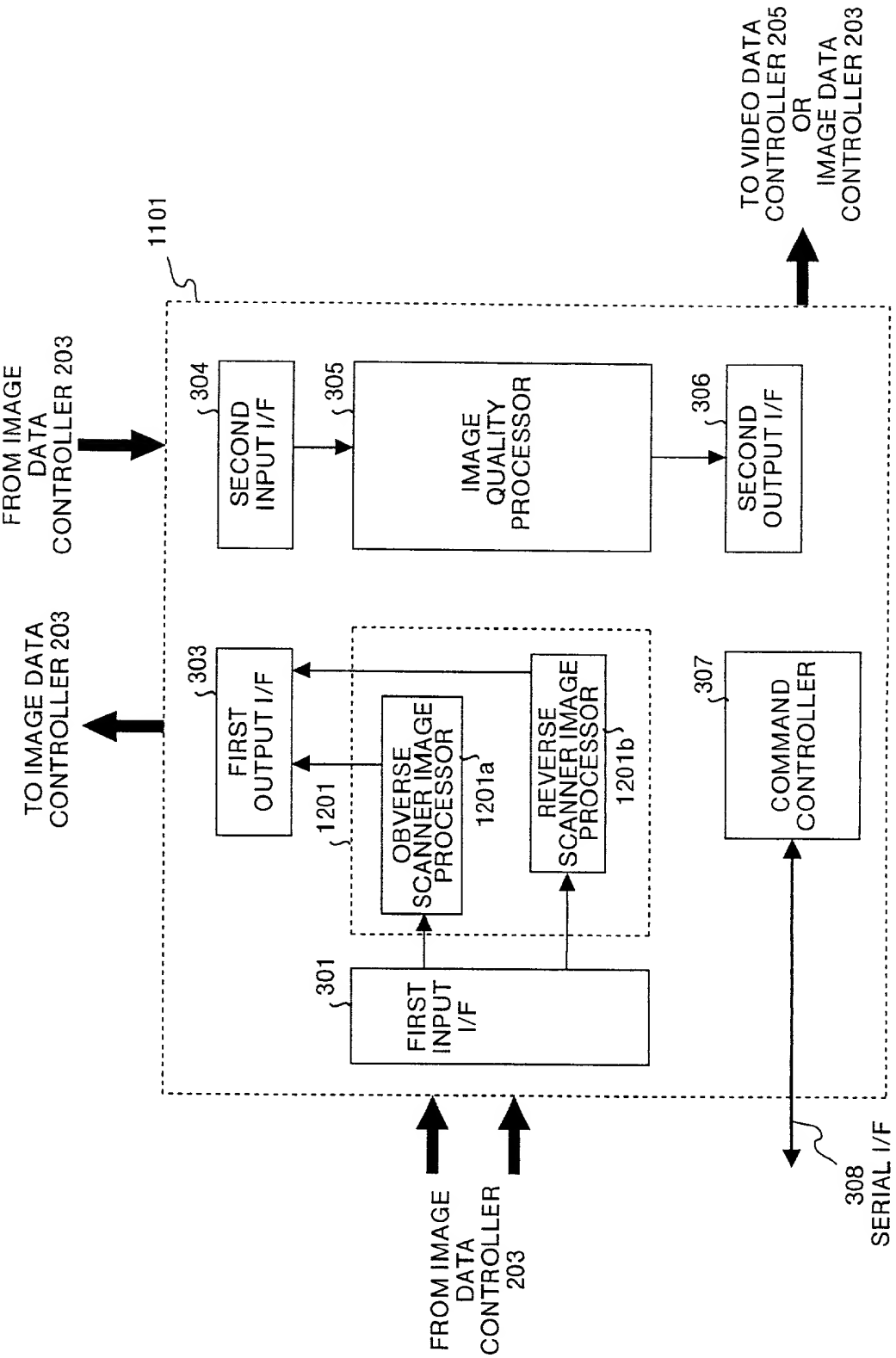
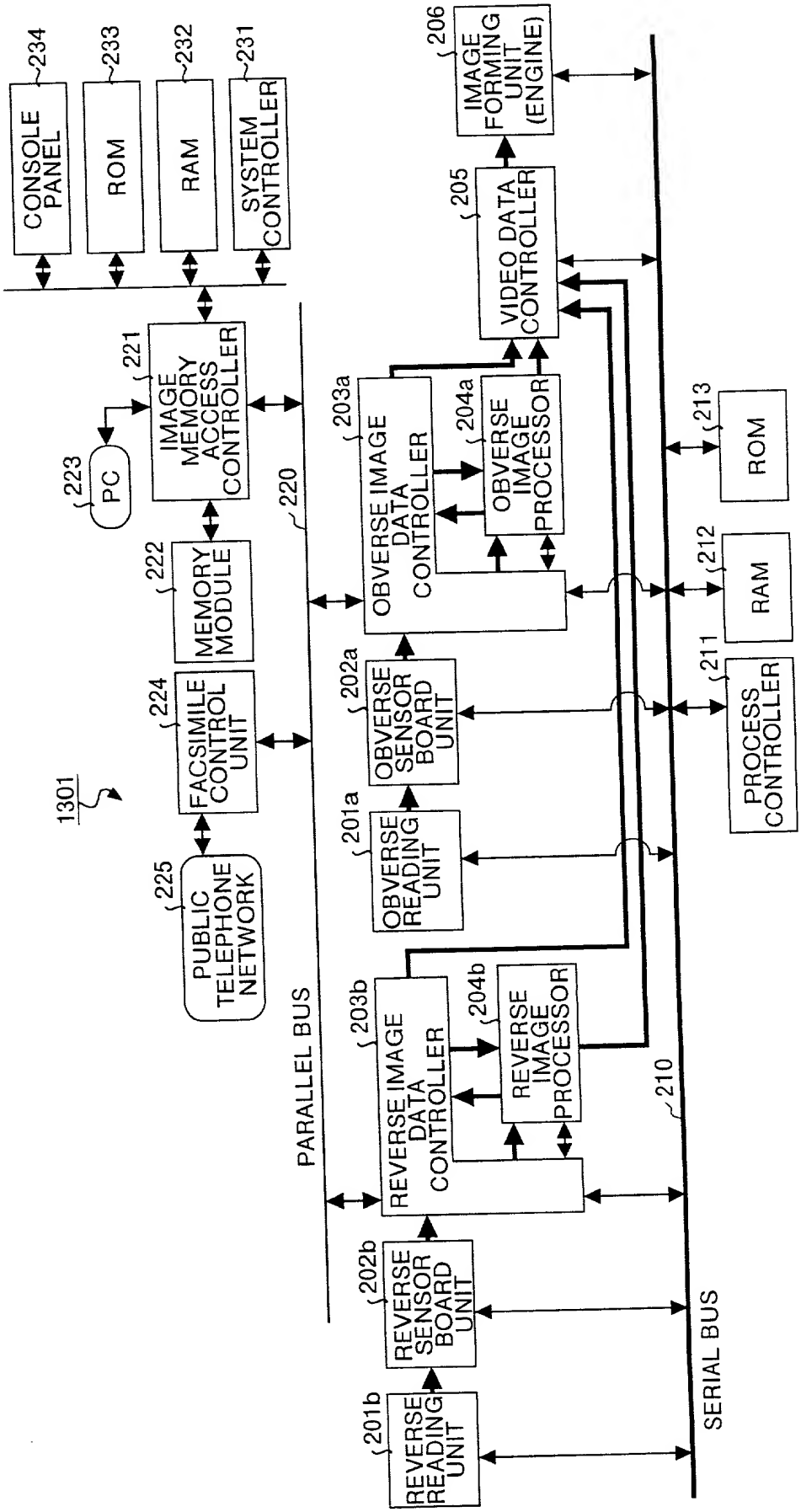

1101
FROM IMAGE DATA CONTROLLER 203
TO IMAGE DATA CONTROLLER 203
TO VIDEO DATA CONTROLLER 205 OR IMAGE DATA CONTROLLER 203
304
SECOND INPUT I/F
305
IMAGE QUALITY PROCESSOR
306
SECOND OUTPUT I/F
303
FIRST OUTPUT I/F
1201
OBVERSE SCANNER IMAGE PROCESSOR
1201a
REVERSE SCANNER IMAGE PROCESSOR
1201b
307
COMMAND CONTROLLER
301
FIRST INPUT I/F
FROM IMAGE DATA CONTROLLER 203
308
SERIAL I/F

FIG.13


CONSOLE PANEL
234
ROM
233
RAM
232
SYSTEM CONTROLLER
231
IMAGE FORMING UNIT (ENGINE)
206
VIDEO DATA CONTROLLER
205
IMAGE MEMORY ACCESS CONTROLLER
221
PC
223
MEMORY MODULE
222
FACSIMILE CONTROL UNIT
224
PUBLIC TELEPHONE NETWORK
225
1301
220
OBVERSE IMAGE DATA CONTROLLER
203a
OBVERSE IMAGE PROCESSOR
204a
OBVERSE SENSOR BOARD UNIT
202a
OBVERSE READING UNIT
201a
REVERSE IMAGE DATA CONTROLLER
203b
REVERSE IMAGE PROCESSOR
204b
REVERSE SENSOR BOARD UNIT
202b
REVERSE READING UNIT
201b
ROM
213
RAM
212
PROCESS CONTROLLER
211
PARALLEL BUS
210
SERIAL BUS

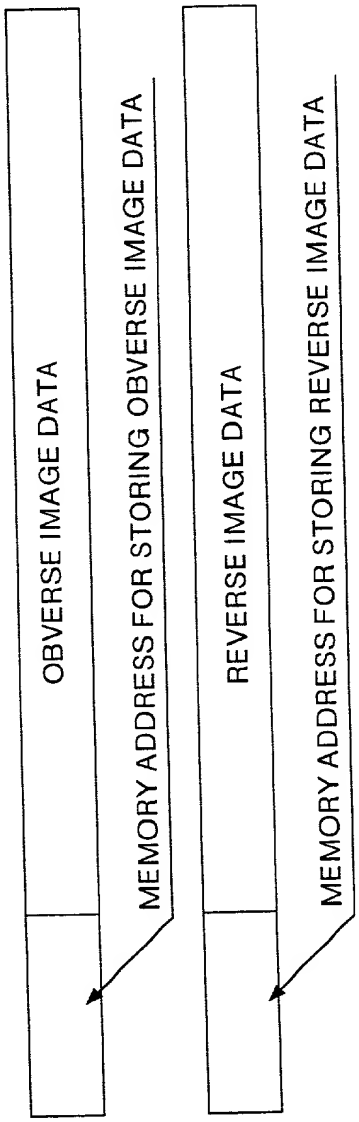


FIG.14A

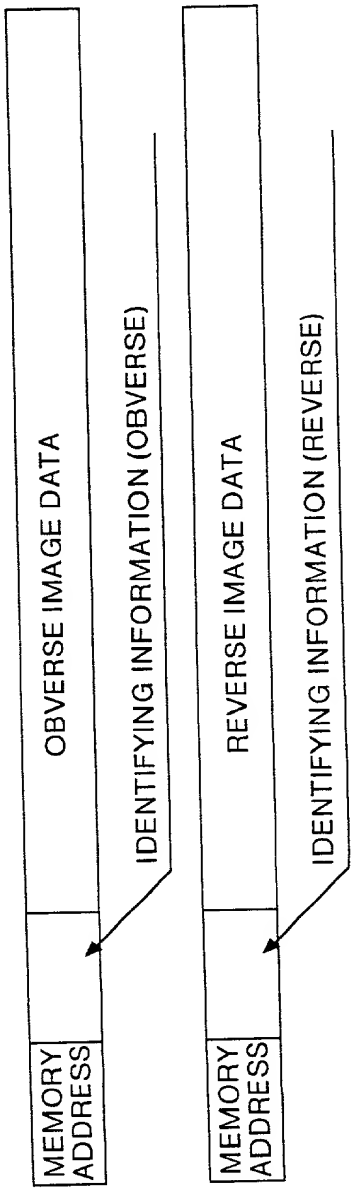


FIG.14B

FIG.15

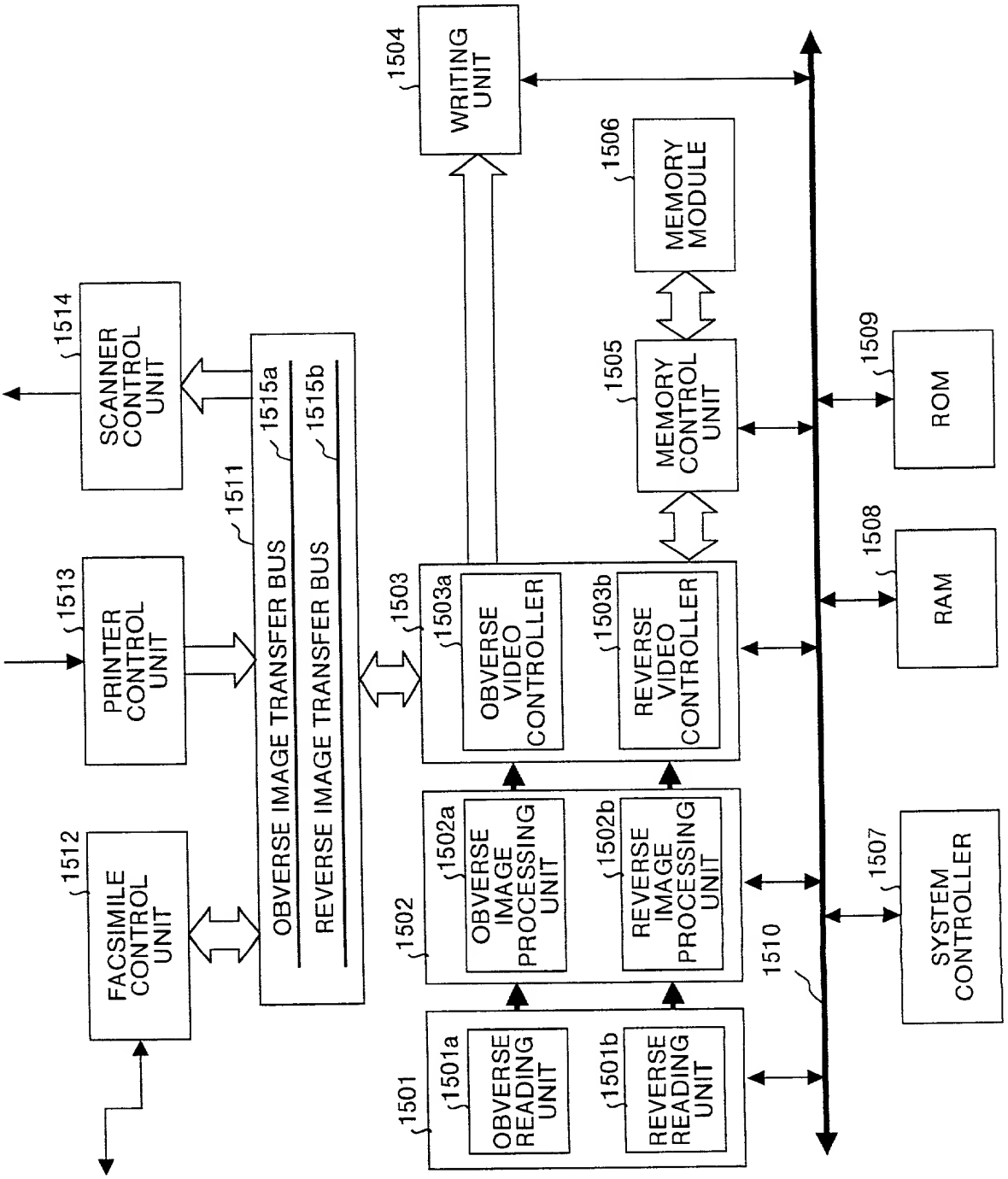

1501
1501a
OBVERSE READING UNIT
1501b
REVERSE READING UNIT
1502
1502a
OBVERSE IMAGE PROCESSING UNIT
1502b
REVERSE IMAGE PROCESSING UNIT
1503
1503a
OBVERSE VIDEO CONTROLLER
1503b
REVERSE VIDEO CONTROLLER
1504
WRITING UNIT
1505
MEMORY CONTROL UNIT
1506
MEMORY MODULE
1507
SYSTEM CONTROLLER
1508
RAM
1509
ROM
1510
1511
OBVERSE IMAGE TRANSFER BUS
1515a
REVERSE IMAGE TRANSFER BUS
1515b
1512
FACSIMILE CONTROL UNIT
1513
PRINTER CONTROL UNIT
1514
SCANNER CONTROL UNIT

FIG.16

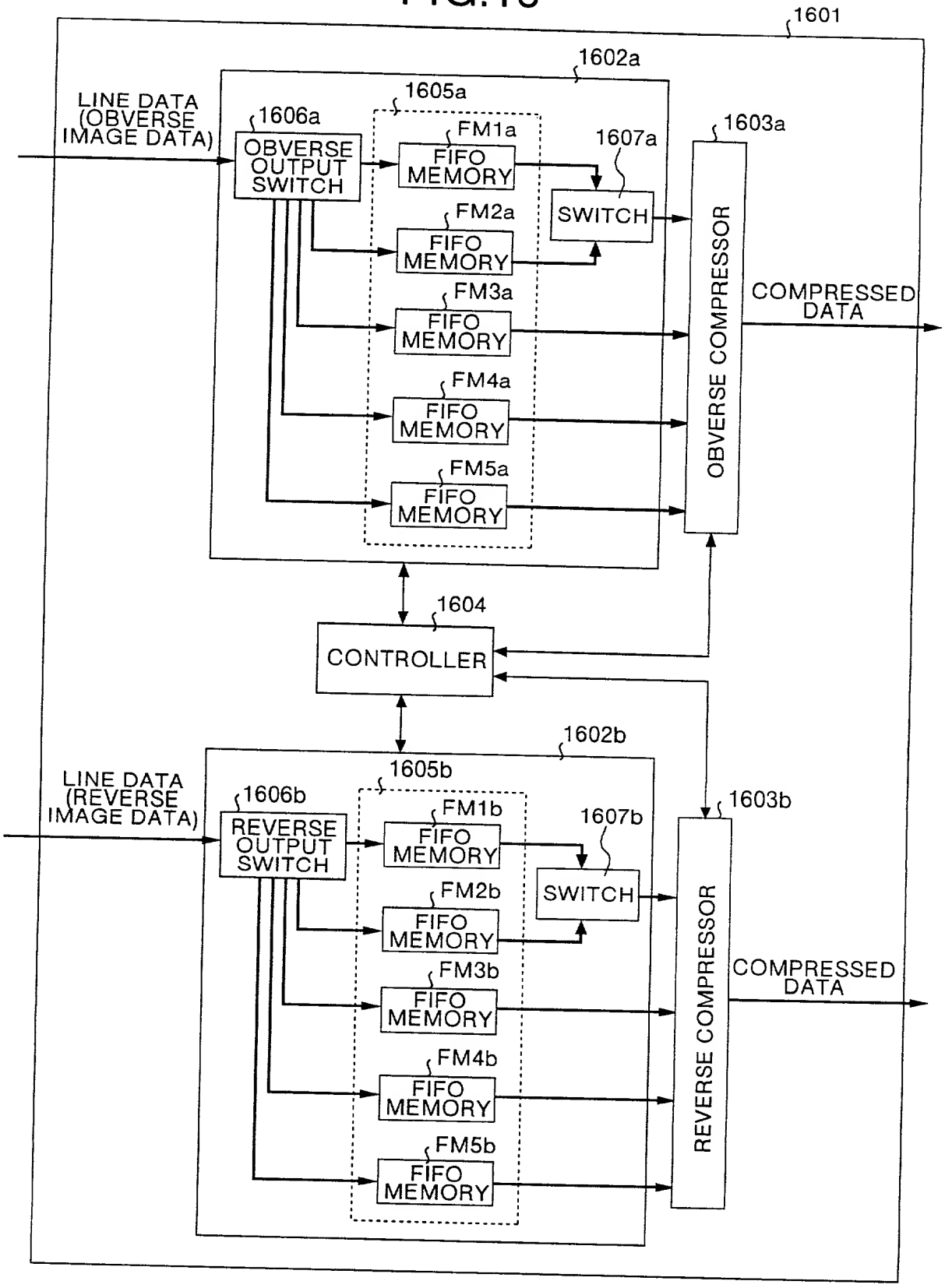

1601
1602a
1605a
LINE DATA (OBVERSE IMAGE DATA)
1606a
OBVERSE OUTPUT SWITCH
FM1a
FIFO MEMORY
1607a
SWITCH
1603a
FM2a
FIFO MEMORY
FM3a
FIFO MEMORY
COMPRESSED DATA
OBVERSE COMPRESSOR
FM4a
FIFO MEMORY
FM5a
FIFO MEMORY
1604
CONTROLLER
1602b
1605b
LINE DATA (REVERSE IMAGE DATA)
1606b
REVERSE OUTPUT SWITCH
FM1b
FIFO MEMORY
1607b
SWITCH
1603b
FM2b
FIFO MEMORY
FM3b
FIFO MEMORY
COMPRESSED DATA
REVERSE COMPRESSOR
FM4b
FIFO MEMORY
FM5b
FIFO MEMORY

FIG.17

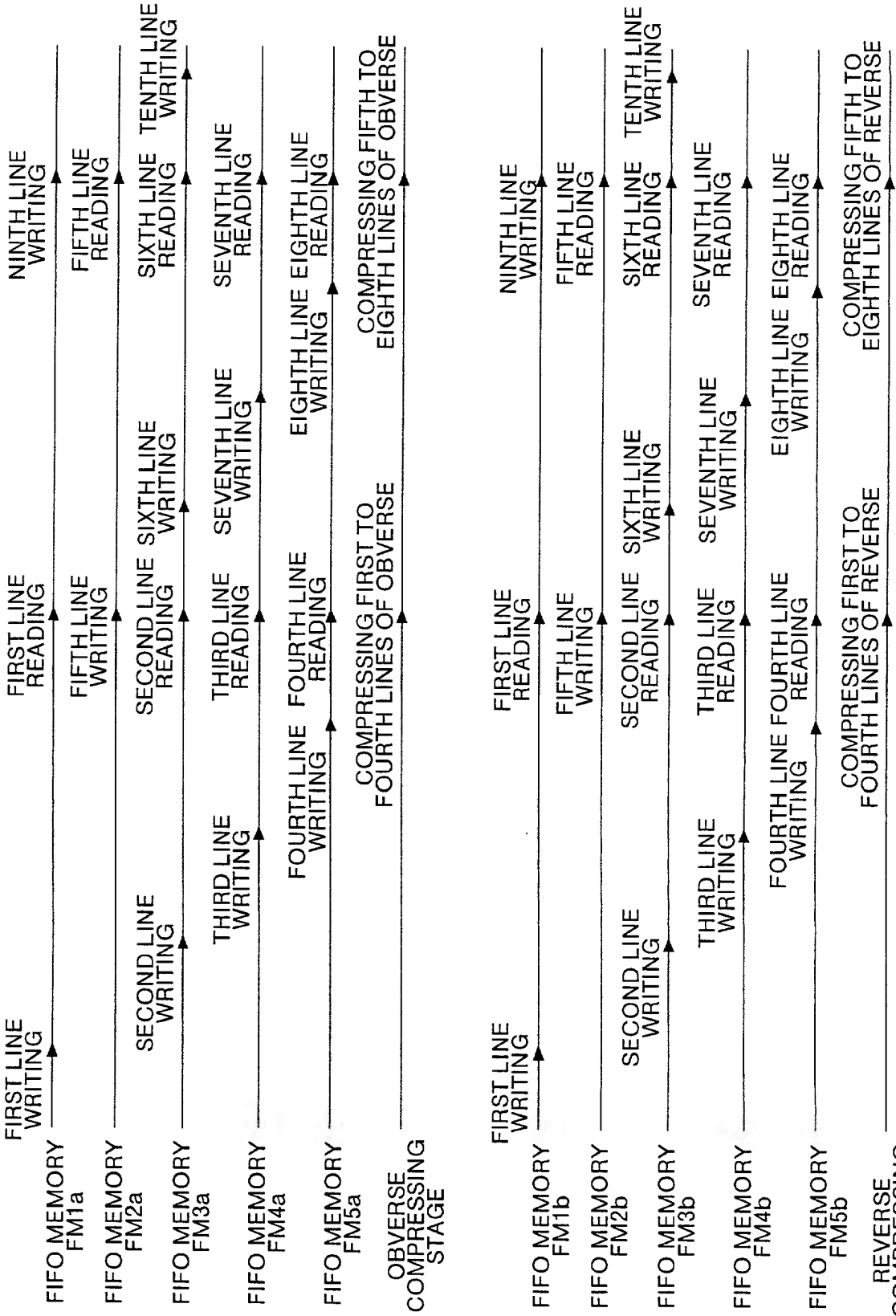
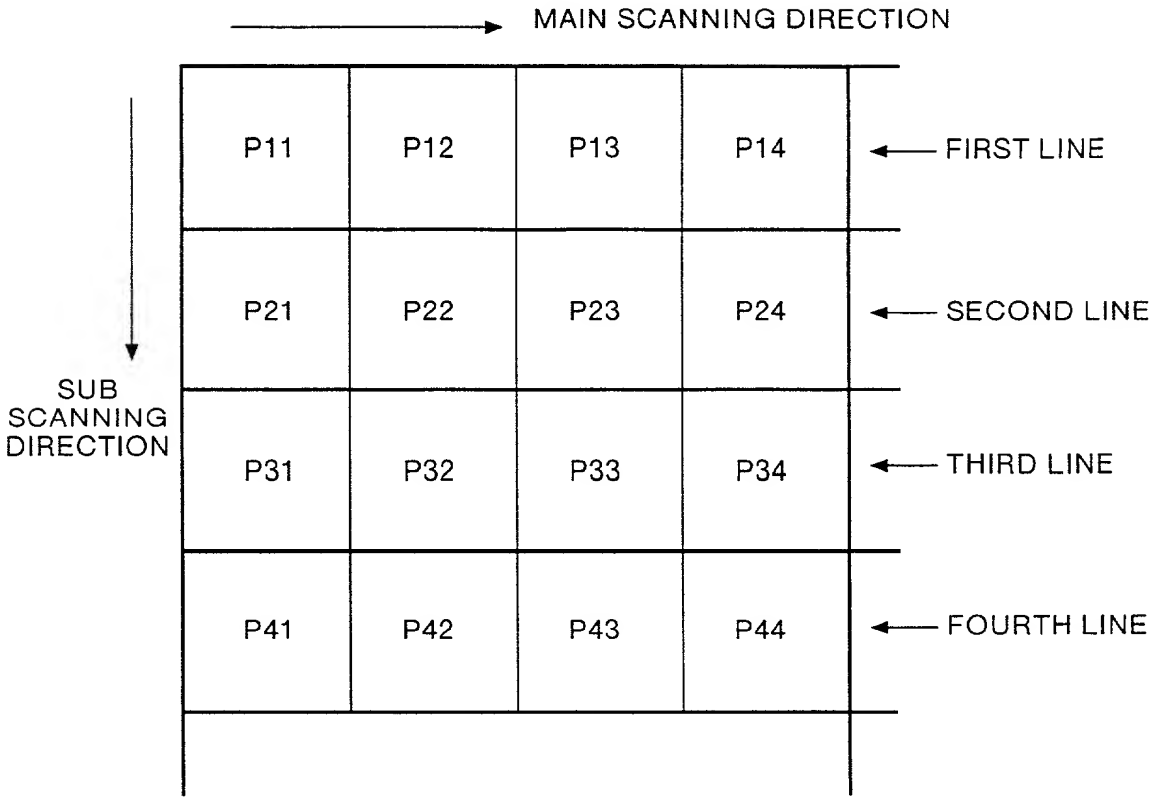

FIFO MEMORY FM1a
FIRST LINE WRITING
FIRST LINE READING
NINTH LINE WRITING
FIFO MEMORY FM2a
FIFTH LINE WRITING
FIFTH LINE READING
FIFO MEMORY FM3a
SECOND LINE WRITING
SECOND LINE READING
SIXTH LINE WRITING
SIXTH LINE READING
TENTH LINE WRITING
FIFO MEMORY FM4a
THIRD LINE WRITING
THIRD LINE READING
SEVENTH LINE WRITING
SEVENTH LINE READING
FIFO MEMORY FM5a
FOURTH LINE WRITING
FOURTH LINE READING
EIGHTH LINE WRITING
EIGHTH LINE READING
OBVERSE COMPRESSING STAGE
COMPRESSING FIRST TO FOURTH LINES OF OBVERSE
COMPRESSING FIFTH TO EIGHTH LINES OF OBVERSE
FIFO MEMORY FM1b
FIRST LINE WRITING
FIRST LINE READING
NINTH LINE WRITING
FIFO MEMORY FM2b
FIFTH LINE WRITING
FIFTH LINE READING
FIFO MEMORY FM3b
SECOND LINE WRITING
SECOND LINE READING
SIXTH LINE WRITING
SIXTH LINE READING
TENTH LINE WRITING
FIFO MEMORY FM4b
THIRD LINE WRITING
THIRD LINE READING
SEVENTH LINE WRITING
SEVENTH LINE READING
FIFO MEMORY FM5b
FOURTH LINE WRITING
FOURTH LINE READING
EIGHTH LINE WRITING
EIGHTH LINE READING
REVERSE COMPRESSING STAGE
COMPRESSING FIRST TO FOURTH LINES OF REVERSE
COMPRESSING FIFTH TO EIGHTH LINES OF REVERSE
LAPSE OF TIME

FIG.18


MAIN SCANNING DIRECTION
SUB SCANNING DIRECTION
P11
P12
P13
P14
FIRST LINE
P21
P22
P23
P24
SECOND LINE
P31
P32
P33
P34
THIRD LINE
P41
P42
P43
P44
FOURTH LINE